Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (currently amended) An apparatus for storing predicted return addresses of instructions being executed by a pipelined processor, the apparatus comprising:

a two part return address buffer, comprising

a speculative return address buffer; and

a committed return address buffer, both of which having multiple entries that may include predicted return addresses that have been pushed onto the return buffer;

wherein the speculative return address buffer comprises a circular buffer including a back pointer field to store pointers into the two part return address buffer.

2. (currently amended) The apparatus of claim 1 wherein when a predicted return address stored in the two part return address buffer is popped, the predicted return address may come from either the speculative return address buffer or the committed return address buffer.

3. (cancelled)

4. (currently amended) The apparatus of claim 2 further comprising:

a read pointer ~~pointing to a first entry in the speculative buffer~~; and

a write pointer ~~pointing to a second entry in the speculative buffer~~;

~~a processor that executes instructions~~ wherein the two part return address buffer is operable to:

store a first return address in an entry in the speculative return address buffer, the entry being pointed to by the write pointer;

store a value of the read pointer in the back pointer field of the entry;

set the read pointer equal to the write pointer; and

increment the write pointer

~~read the first return address from the entry in the first set of entries, the entry being pointed to by the read pointer~~.

5. (cancelled)

6. (cancelled)

7. (currently amended) The apparatus of claim 4 ~~6~~, further comprising:

a storage device holding an SCOLOR indicator bit that is inverted each time the read pointer wraps over or under a depth N of the speculative buffer ~~is set to point to the first or last entry in the speculative buffer~~; and

a bit storage location associated with each entry in the speculative buffer to hold ~~the~~ a current value of SCOLOR each time a return address is written into the speculative buffer.

8. (currently amended) The apparatus of claim 4, further comprising ~~comprises~~:

retirement logic ~~connected to the apparatus~~ that indicates instructions that have completed execution in the processor, wherein when the retirement logic indicates an instruction has completed execution the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.

9. (original) The apparatus of claim 4, further comprising:

a storage location holding a pointer indicator bit to indicate the use of the speculative buffer or the committed buffer for reading a return address.

10. (currently amended) The apparatus of claim 9, wherein the two part return address buffer is operable to, when the pointer indicator bit indicates the speculative buffer is to be used for reading the return address, read the return address ~~is read~~ from the speculative buffer and set the read pointer ~~is set~~ equal to a value of the back pointer field of an ~~back address from the~~ entry being read.

11. (currently amended) The apparatus of claim 10, further comprising:

a retirement logic block ~~connected to the apparatus~~ that indicates instructions that have completed execution in the processor,

wherein when the retirement logic indicates a CALL instruction has completed execution, the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.

12-19. (cancelled)

20. (currently amended) A method of storing predicted return addresses of instructions being executed by a pipelined processor, the method comprising:

pushing a return address onto a two part return address buffer, wherein the two part buffer comprises a speculative return address buffer and a committed return address buffer, both of which having multiple entries; and

popping the predicted return address from the two part buffer, wherein the popped return address may come from either the speculative return address buffer or the committed address buffer;

wherein the speculative return address buffer comprises a circular buffer including a back pointer field to store pointers into the two part return address buffer.

21. (original) The method of claim 20, further comprising:

popping a return address from the committed buffer to allow recovery of predicted RETURN addresses in the case of mis-predicted instruction fetching.

22. (currently amended) The method of claim 21, further comprising:

storing a first return address in an entry in the speculative buffer, the entry being pointed to by ~~the~~ a write pointer; and

reading the first return address from the entry ~~in the first set of entries~~, the entry being pointed to by ~~the~~ a read pointer.

23. (currently amended) The method of claim 21, wherein pushing a return address onto the speculative buffer comprises:

storing a value of a ~~the~~ read pointer ~~as a~~ in the back pointer field ~~in the same entry~~;

setting the read pointer equal to ~~the value of the~~ a write pointer; and

incrementing the write pointer after the read pointer is set equal to the write pointer.

24. (cancelled)

25. (currently amended) The method of claim 21 ~~24~~, further comprising:

inverting [[a]] an SCOLOR indicator bit each time a ~~the~~ read pointer wraps over or under a depth N of the speculative buffer ~~is set to point to the first or last entry in the speculative buffer~~; and

storing the SCOLOR indicator bit in an associated bit location each time a return address is written into the speculative buffer.

26. (currently amended) The method of claim 21~~-22~~, wherein upon an indication that an instruction corresponding to a return address stored in the two part buffer has completed execution, the method further comprises:

writing the return address corresponding to the completed instruction from the speculative buffer to the committed buffer.

27. (currently amended) The method of claim 21~~-22~~, further comprising, ~~wherein~~ when a pointer indicator bit indicates the speculative buffer is to be used for reading the return address~~, the instructions cause a machine to~~:

reading the return address from the speculative buffer; and

setting the read pointer equal to a value of the back pointer field of an ~~address from the~~ entry being read.

28. (new) A system comprising:

a super-scalar, pipelined processor; and

a two part return address buffer comprising a speculative return address buffer and a committed return address buffer, both of which having multiple entries that may include predicted return addresses that have been pushed onto the two part return address buffer;

wherein the speculative return address buffer comprises a circular buffer including a back pointer field to store pointers into the two part return address buffer.

29. (new) The system of claim 28 wherein when a predicted return address stored in the two part return address buffer is popped, the predicted return address may come from either the speculative return address buffer or the committed return address buffer.

30. (new) The system of claim 29 further comprising:

a read pointer; and

a write pointer;

wherein the two part return address buffer is operable to:

store a first return address in an entry in the speculative return address buffer, the entry being pointed to by the write pointer;

store a value of the read pointer in the back pointer field of the entry;

set the read pointer equal to the write pointer; and

increment the write pointer.

31. (new) The system of claim 30, further comprising:

a storage device holding an SCOLOR indicator bit that is inverted each time the read pointer wraps over or under a depth N of the speculative buffer; and

a bit storage location associated with each entry in the speculative buffer to hold a current value of SCOLOR each time a return address is written into the speculative buffer.

32. (new) The system of claim 30, further comprising:

retirement logic that indicates instructions that have completed execution in the processor, wherein when the retirement logic indicates an instruction has completed execution the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.

33. (new) The system of claim 30, further comprising:

a storage location holding a pointer indicator bit to indicate the use of the speculative buffer or the committed buffer for reading a return address.

34. (new) The system of claim 33, wherein the two part return address buffer is operable to, when the pointer indicator bit indicates the speculative buffer is to be used for reading the return address, read the return address from the speculative

buffer and set the read pointer equal to a value of the back pointer field of an entry being read.

35. (new) The system of claim 34, further comprising:

a retirement logic block that indicates instructions that have completed execution in the processor,

wherein when the retirement logic indicates a CALL instruction has completed execution, the return address corresponding to the completed instruction is written from the speculative buffer to the committed buffer.